Academic Course Description

BHARATH UNIVERSITY
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

BEC010 VLSI Design
Fifth Semester (Elective) 2017-18

Course (catalog) description

VLSI Design helps the students to learn basic MOS Circuits and their process technology. The subject also teaches the techniques of chip design using programmable devices and the various concepts of designing VLSI Subsystems.

Compulsory/Elective course : Elective for ECE students
Credit & contact hours : 3 & 45
Course Coordinator : Ms.M.Jasmin, Assoc.Professor

Instructors :

Name of the instructor	Class handling	Office location	Office phone	Email (domain:@ bharathuniv.ac.in	Consultation
Ms.Sheryl Nivya	Third year	SA006		beulahhemalatha.ece	12.30-1.30 pm

Relationship to other courses:

Pre –requisites : Electronics Circuits & Principles of Digital Electronics

Assumed knowledge : The students will have a basic knowledge in Digital electronics and Electron devices.

Following courses : BEC702 Digital CMOS VLSI

Syllabus Contents

UNIT I MOS TRANSISTOR THEORY **9 HOURS**

MOSFET– Enhancement mode & Depletion mode – Fabrication – NMOS, PMOS – CMOS fabrication – P-well, N-well, Twin-Tub, SOI – BiCMOS Technology –Comparison with CMOS.

UNIT II MOS CIRCUITS AND DESIGN **9 HOURS**

Basic Electrical properties of MOS circuits – DC Equations, NMOS & CMOS inverter –Second Order Effects– Basic circuit concepts-Sheet resistance-Area Capacitances-Capacitance calculations-Inverter delays–Scaling of MOS Devices –Scaling Models and Scaling Factors-MOS layers – Stick diagram – NMOS Design Style – CMOS Design style – lambda based design rules– Simple Layout examples

UNIT III SUBSYSTEM DESIGN & LAYOUT **9 HOURS**

Switch Logic – Pass transistors and transmission gates – Two input NMOS, CMOS gates: NOT– NAND– NOR gates – Other forms of CMOS logic – Static CMOS logic-Dynamic CMOS logic – Clocked CMOS logic - Precharged domino CMOS logic – Structured design of simple Combinational logic design– Multiplexers – Clocked sequential circuits – Two phase clocking – D-Flip-flop-Charge storage - Dynamic register element –Dynamic shift register

UNIT IV PROGRAMMABLE LOGIC DEVICES **9 HOURS**

Programmable Logic Devices – PLA , PAL – Finite State Machine design using PLA – Introduction to FPGA – FPGA Design flow –Architecture – FPGA devices: Xilinx XC 4000 – Altera cyclone III

UNIT V VERILOG HDL DESIGN PROGRAMMING **9 HOURS**

Basic concepts: VLSI Design flow, Modeling, Syntax and Programming, Design Examples:Combinational Logic – Multiplexer, Decoder/Encoder, Comparator, Adders, Multipliers, Sequential logic- Flip Flops, Registers, and Counters, Memory- Introduction to back end tools.

REFERENCES:

1.Douglas A.Pucknell, K. Eshragian,—Basic VLSI Design , Third edition,PHI,2009

2.Neil.H.E.Weste,KamaranEshraghian,—PrinciplesofCMOSVLSIDesign,Second Edition, AddisoWesleyPublications,2002

3.SamirPalnitkar,—VerilogHDL–GuidetoDigitaldesignandsynthesis, SecondEdition Pearson Education,2009

4.WayneWolf, —ModernVLSIDesign, PearsonEducation , 2003

5.https://en.wikipedia.org/wiki/Very-large-scale_integration

Computer usage: HDL simulation and tool, viz., Modelsim.

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Broad area : Communication | Signal Processing | Electronics | **VLSI** | Embedded

Test Schedule

S. No.	Test	Tentative Date	Portions	Duration
1	Cycle Test-1	August 1st week	Session 1 to 14	2 Periods
2	Cycle Test-2	September 2nd week	Session 15 to 28	2 Periods
3	Model Test	October 2nd week	Session 1 to 45	3 Hrs
4	University Examination	TBA	All sessions / Units	3 Hrs.

Mapping of Instructional Objectives with Program Outcome

The goals of the course is to ensure that the learners become familiar	Correlates to program outcome		
	H	M	L
Identify the various IC fabrication methods.	c	d	e
Express the Layout of simple MOS circuit using Lambda based design rules.	d	e	c
Apply the Lambda based design rules for subsystem design.	b	c	e
Differentiate various FPGA architectures.	e	c	d
Design an application using Verilog HDL.	c	k	e
Concepts of modeling a digital system using Hardware Description Language.	c	k	e

H: high correlation, M: medium correlation, L: low correlation

Draft Lecture Schedule

Session	Topics	Problem solving (Yes/No)	Text / Chapter
UNIT I MOS TRANSISTOR THEORY			
1.	MOSFET– Enhancement mode, Depletion mode	No	[R1] Chapter -1
2.	Fabrication- NMOS- P-well,	No	
3.	Fabrication- NMOS- N-well, Twin-Tub	No	
4.	Fabrication- PMOS	No	
5.	Fabrication- CMOS	No	
6.	BiCMOS Technology	No	
7.	Comparison with CMOS.	No	
UNIT II MOS CIRCUITS AND DESIGN			
8.	Basic Electrical properties of MOS circuits – DC Equations, Inverter delays	No	[R1] Chapter -2,3,5
9.	NMOS & CMOS inverter	No	
10.	Second Order Effects	No	
11.	Basic circuit concepts	No	
12.	Sheet resistance-Area Capacitances-Capacitance calculations	No	
13.	Scaling of MOS Devices	No	
14.	Scaling Models and Scaling Factors	No	
15.	MOS layers – Stick diagram	No	
16.	NMOS Design Style – CMOS Design style	No	
17.	Lambda based design rules– Simple Layout examples	No	

UNIT III SUBSYSTEM DESIGN & LAYOUT			
18.	Switch Logic – Pass transistors and transmission gates	No	[R2] Chapter -6
19.	Two input NMOS, CMOS gates: NOT– NAND– NOR gates	No	
20.	Other forms of CMOS logic – Static CMOS logic	No	
21.	Dynamic CMOS logic	No	
22.	Clocked CMOS logic	No	
23.	Precharged domino CMOS logic	No	
24.	simple Combinational logic design– Multiplexers	No	
25.	Structured design of– Clocked sequential circuits	No	
26.	Two phase clocking – D-Flip-flop-Charge storage	No	
27.	Dynamic register element –Dynamic shift register	No	
UNIT IV PROGRAMMABLE LOGIC DEVICES			
28.	Programmable Logic Devices	No	[R2] Chapter -10
29.	Programmable Logic Array (PLA)	No	
30.	Programmable Array Logic (PAL)	No	
31.	Finite State Machine design using PLA	No	
32.	Introduction to FPGA	No	
33.	FPGA Design flow	No	
34.	FPGA Architecture	No	
35.	FPGA devices: Xilinx XC 4000	No	
36.	Altera cyclone III	No	
UNIT V VERILOG HDL DESIGN PROGRAMMING			
37.	Basic concepts: VLSI Design flow	No	[R3] Chapter -1,3
38.	Modeling, Syntax and Programming	No	
39.	Design Examples: Combinational Logic – Multiplexer	No	
40.	Decoder/Encoder	No	
41.	Comparator	No	
42.	Adders, Multipliers	No	
43.	Sequential logic- Flip Flops, Registers	No	
44.	Counters, Memory	No	
45.	Introduction to back end tools.	No	

Teaching Strategies

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures
- Tutorials, which allow time for students to resolve various programs in Verilog for understanding of lecture material.
- Laboratory sessions, which support the formal lecture material and also provide the student with practical construction, measurement and debugging skills.
- Small periodic quizzes, to enable you to assess your understanding of the concepts.

Evaluation Strategies

Cycle Test – I	-	5%
Cycle Test – II	-	5%
Model Test	-	10%
Assignment /Seminar/online test/quiz	-	5%
Attendance	-	5%
Final exam	-	70%

Prepared by: Ms.M.Jasmin, Assoc.Professor **Dated :**

Addendum

ABET Outcomes expected of graduates of B.Tech / ECE / program by the time that they graduate*:*

a. An ability to apply knowledge of mathematics, science, and engineering

b. An ability to design and conduct experiments, as well as to analyze and interpret data

c. An ability to design a hardware and software system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability

d. An ability to function on multidisciplinary teams

e. An ability to identify, formulate, and solve engineering problems

f. An understanding of professional and ethical responsibility

g. An ability to communicate effectively

h. The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context

i. A recognition of the need for, and an ability to engage in life-long learning

j. A knowledge of contemporary issues

k. An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Program Educational Objectives

PEO1: PREPARATION

Electronics Engineering graduates are provided with a strong foundation to passionately apply the fundamental principles of mathematics, science, and engineering knowledge to solve technical problems and also to combine fundamental knowledge of engineering principles with modern techniques to solve realistic, unstructured problems that arise in the field of Engineering and non-engineering efficiently and cost effectively.

PEO2: CORE COMPETENCE

Electronics engineering graduates have proficiency to enhance the skills and experience to apply their engineering knowledge, critical thinking and problem solving abilities in professional engineering practice for a wide variety of technical applications, including the design and usage of modern tools for improvement in the field of Electronics and Communication Engineering.

PEO3: PROFESSIONALISM

Electronics Engineering Graduates will be expected to pursue life-long learning by successfully participating in post graduate or any other professional program for continuous improvement which is a requisite for a successful engineer to become a leader in the work force or educational sector.

PEO4: SKILL

Electronics Engineering Graduates will become skilled in soft skills such as proficiency in many languages, technical communication, verbal, logical, analytical, comprehension, team building, interpersonal relationship, group discussion and leadership ability to become a better professional.

PEO5: ETHICS

Electronics Engineering Graduates are morally boosted to make decisions that are ethical, safe and environmentally-responsible and also to innovate continuously for societal improvement.

Course Teacher	Signature
Ms. M.JASMIN	
Ms.S.BEULAH HEMALATHA	

Course Coordinator **HOD/ECE**